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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/756,863

Applicant(s)

YOSHIDA, TOYOHICO

Examiner

Barry J. O'Brien

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12, 14, 16, 18 and 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14, 16, 18 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-12, 14, 16, 18 and 19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 3/15/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 12, 14, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Emma, U.S. Patent No. 5,619,665.

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7. Regarding claim 1, Emma has taught in a processor (608 of Fig.6) operating with instructions in a first instruction architecture as a native instruction, an instruction translator used with an instruction memory to store an instruction in a second instruction architecture different from said first instruction architecture, for translating an instruction in said second instruction architecture into an instruction in said first instruction architecture for application to said processor (see Col.3 lines 2-17), said instruction translator comprising;

- a. A translator (606 of Fig.6) for reading out an instruction from said instruction memory (602 of Fig.6) in response to a received first address in said instruction memory of an instruction to be executed by said processor and translating the read out instruction in said second instruction architecture into an instruction in said first instruction architecture (see Col.12 lines 42-56),
- b. An instruction cache (604 of Fig.6) for temporarily holding the instruction in said first instruction architecture after the translation by said translator in association with the first address in said instruction memory (see Col.12 lines 51-56),
- c. A selector for searching said instruction cache in response to a received second address of an instruction to be executed by said processor, and for selectively outputting, based on a determination result of whether or not an instruction corresponding to the instruction of the second address is held in said instruction cache, an instruction output by said translator and the corresponding instruction held in said instruction cache (see Col.12 line 59 – Col.12 line 6).

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8. Regarding claim 12, Emma has taught an instruction memory attached with a translator, used with a processor operating with an instruction in a first instruction architecture as a native instruction (see Col.3 lines 2-17), comprising:

- a. An instruction storage unit (602 of Fig.6) to store an instruction in a second instruction architecture (see Col.12 lines 42-49),
- b. An instruction translator (606 of Fig.6) to translate an instruction in said second instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor (see Col.12 lines 42-56), said instruction translator including:
 - I. A translator (606 of Fig.6) to read out the instruction in said second instruction architecture from said instruction storage unit (602 of Fig.6) in response to a received first address of an instruction to be executed by said processor and translate the read out instruction in said second instruction architecture in the instruction in said first instruction architecture (see Col.12 lines 42-56),
 - II. An instruction cache (604 of Fig.6) to temporarily hold the instruction in said first instruction architecture after the translation by said translator in association with the first address (see Col.12 lines 51-56),
 - III. A selector to search said instruction cache in response to a received second address of an instruction to be executed by said processor and selectively output to said processor, based on a determination result of whether or no an instruction corresponding to the instruction of the address is held in

said instruction cache, and instruction output by said translator and the corresponding instruction in said first instruction architecture held in said instruction cache (see Col.12 line 59 – Col.13 line 6).

9. Regarding claim 14, Emma has taught the instruction memory attached with a translator according to claim 12, further comprising an address translator to translate an address at the time of reading from said instruction storage unit (see Col.11 lines 4-13). Here, Emma has taught the address of source instructions A, B, and C being translated to a native instruction X_1 having the address of source instruction A, the translating the addresses of B and C to be the address of A (X_1).

10. Regarding claim 16, Emma has taught a data processing apparatus, comprising:

- a. A processor (608 of Fig.6) operating with an instruction in a first instruction architecture as a native instruction (see Col.3 lines 2-17),
- b. A bus (612 of Fig.6) to which said processor is connected,
- c. A first instruction memory (602 of Fig.6) with a translator (606 of Fig.6) interconnected with said processor through said bus,
- d. A second instruction memory (604 of Fig.6) interconnected to said processor through said bus,
- e. Said first instruction memory with a translator including:
 - I. A first instruction storage unit (602 of Fig.6) to store an instruction in a second instruction architecture transferred from said processor through said bus (see Col.12 lines 42-49),

- II. An instruction translator to translate the instruction in said second instruction architecture output from said first instruction storage unit into an instruction in said first instruction architecture for application to said processor through said bus (see Col.12 lines 42-56),
- f. Said second instruction memory including:
 - I. A second instruction storage unit (604 of Fig.6) to store an instruction in said first instruction architecture transferred from said processor through said bus (see Col.12 lines 51-56),
 - II. An instruction reading circuit responsive to an address signal applied from said processor through said bus for applying an instruction in said first instruction architecture output from said second instruction storage unit to said processor through said bus (see Col.12 line 59 – Col.13 line 6).
- 11. Regarding claim 18, Emma has taught the data processing apparatus according to claim 16, wherein the number of clock cycles spent by said processor to access said first instruction memory through said bus is larger than the number of clock cycles spent by said processor to access said second instruction memory through said bus (see Col.12 lines 59-67 and Col.13 lines 1-6). Here, when an instruction is read out of the first instruction memory, it needs to be translated. But because when reading out of the second instruction memory the instruction has already been translated (see Col.12 lines 65-67 and Col.13 lines 1-6), it is inherent that it will take less time to read out from an instruction memory that does not have to perform a translation.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S.

Patent No. 5,619,665 as applied to claim 1 above, and further in view of Dickol et al., U.S.

Patent No. 5,875,336.

14. Regarding claim 2, Emma has taught the instruction translator according to claim 1, but has not explicitly taught wherein said second instruction architecture is a variable length instruction architecture, and said translator includes a variable length translator for translating an instruction in said second instruction architecture read out from said instruction memory into one or more instruction in said first instruction architecture, the number of which depends on an instruction length of the read out instruction in said second instruction architecture.

15. However, Dickol has taught a variable length instruction architecture being translated in real time into one or more instructions of a second instruction architecture based on the varying lengths of instructions in the variable length instruction architecture (see Dickol, Col.3 lines 29-38 and Col.4 lines 13-14, 21-27) in order to improve performance when executing non-native instructions on more common native-instruction-based hardware (see Dickol, Col.1 lines 47-61 and Col.2 lines 15-18). One of ordinary skill in the art would have recognized that a priority of microprocessor designers is to improve performance while minimizing cost and hardware complexity. Therefore, one of ordinary skill in the art at the time of the invention would have

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found it obvious to modify Emma to further decode instructions from a non-native variable length instruction set into one or more native instructions in order to improve processor performance when executing non-native instructions while minimizing the additional hardware required to do so.

16. Regarding claim 3, Emma in view of Dickol has taught the instruction translator according to claim 2, wherein said variable length translator translates the instruction in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture having a total length depending on and larger than the instruction length of said read out instruction in said second instruction architecture (see Dickol, Col.3 lines 29-38 and Col.4 lines 13-14, 21-27).

17. Claims 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Dickol et al., U.S. Patent No. 5,875,336 as applied to claims 1-3 above, and further in view of Goettelmann et al., U.S. Patent No. 5,313,614.

18. Regarding claim 4, Emma in view of Dickol have taught the instruction translator according to claim 3, but have not explicitly taught wherein each instruction in said first instruction architecture includes one or a plurality of sub instructions, and the number of the sub instructions included in the instruction in the first instruction architecture translated by said variable length translator depends on the instruction length of said read out instruction in said second instruction architecture.

19. However, Goettelmann has taught the translation from a source instruction architecture (see "source machine code" of Fig.11) into a native instruction architecture (see "translated code" of Fig.11), wherein the native architecture contains a plurality of sub-instructions (see

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“expanded intermediate language code” of Fig.11), sub-instructions which can then be removed if necessary in order to reduce the translated code size (see Col.4 lines 6-18). One of ordinary skill in the art would have recognized that it is desirable to reduce the size of instruction code so that less hardware (memory space) is needed, thus lowering costs. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction translator of Emma in view of Dickol to further translate instructions from a source architecture into a native architecture that includes a plurality of sub-instructions in order to reduce the amount of instruction storage required to store the translated code. Furthermore, because the number of native instructions are dependent on the length of the varying-length source instruction as shown above, and because the number of sub instructions depend on the native instructions, then the number of sub-instructions depend on the length of the source instructions.

20. Regarding claim 6, Emma in view of Dickol has taught the instruction translator according to claim 1, but have not explicitly taught wherein:

- a. Each instruction in said first instruction architecture can include one or a plurality of sub instructions,
- b. Said translator translates a plurality of instructions in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture including sub instructions, the number of which depends on the number of said plurality of instructions.

21. However, However, Goettelmann has taught the translation from a source instruction architecture (see “source machine code” of Fig.11) into a native instruction architecture (see “translated code” of Fig.11), wherein the native architecture contains a plurality of sub-

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instructions (see “expanded intermediate language code” of Fig. 11), sub-instructions which can then be removed if necessary in order to reduce the translated code size (see Col. 4 lines 6-18).

One of ordinary skill in the art would have recognized that it is desirable to reduce the size of instruction code so that less hardware (memory space) is needed, thus lowering costs. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction translator of Emma in view of Dickol to further translate instructions from a source architecture into a native architecture that includes a plurality of sub-instructions in order to reduce the amount of instruction storage required to store the translated code. Furthermore, because the number of native instructions are dependent on the length of the varying-length source instruction as shown above, and because the number of sub instructions depend on the native instructions, then the number of sub-instructions depend on the length of the source instructions.

22. Regarding claim 7, Emma in view of Dickol in further view of Goettelmann have taught the instruction translator according to claim 6, wherein the number of sub instructions included in the instruction in said first instruction architecture after said translation is equal to the number of said plurality of instructions (see “BEQ Label instruction” of “source machine code”, its corresponding “BFALSE FlagZ, Label” instruction of “translated code”, with associated sub-instruction “BFALSE FlagZ, Label” of “expanded intermediate language code”, all of Fig. 11 of Goettelmann).

23. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Gregor, U.S. Patent No. 5,023, 776.

24. Regarding claim 8, Emma has taught the instruction translator according to claim 1 as shown above, wherein:

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- a. Said translator translates said read out instruction in said second instruction architecture into one or a plurality of instructions as the instruction in said first instruction architecture (see Col.12 lines 42-56)

25. Emma has not explicitly taught where said instruction translator further comprises a controller for controlling said instruction cache so that said instruction cache holds each of said one or said plurality of instruction held in said instruction cache as an entry which can be invalidated in one of first and second conditions.

26. However, Gregor has taught the holding of a cache line within a cache so that it cannot be replaced until an EOP signal is detected in order to reduce cache busy time and improve processor performance (see Col.22 lines 36-67). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the cache of Emma to hold a plurality of instructions in a cache until an EOP signal is detected. Furthermore, because the claim language is in the alternative format, only one of the two invalidation condition requirements is required to be met, and thus the EOP signal that is detected (see Col.22 lines 56-57 of Gregor) can be considered such a signal.

27. Regarding claim 10, Emma in view of Gregor has taught the instruction translator according to claim 8, wherein said controller outputs a signal asserted when a new instruction cannot be held in said instruction cache without invalidating an entry which can be invalidated in the second condition (see Col.22 lines 36-67).

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28. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Gregor, U.S. Patent No. 5,023, 776, in further view of Schacham et al., U.K. Patent Application GB220481A.

29. Regarding claim 9, Emma in view of Gregor have taught the instruction translator according to claim 8, wherein:

- a. Said first condition is a holding control condition by hardware control based on a prescribed algorithm by said instruction cache (see Col.22 lines 36-67).

30. Emma in view of Gregor has not explicitly taught wherein the said second condition is a condition in which an explicit invalidation instruction is applied from the outside of said instruction cache.

31. However, in the parent claim of claim 9 only one of the two invalidation conditions must be met. Therefore, because Emma in view of Gregor has satisfied one of the conditions, namely the holding control condition as shown above, the claim language is satisfied.

32. Furthermore, even though the alternative form claim language is met, Schacham has taught that a cache invalidation instruction can be executed to invalidate the entire instruction cache or a portion of it (see p.4 lines 28-30) in order to maintain proper cache coherence and provide better processor performance (see p.2 lines 8-23). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction cache of Emma in view of Gregor to allow a cache invalidation instruction to be executed so that cache coherency is maintained and processor performance is improved.

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33. Regarding claim 11, Emma in view of Gregor has taught the instruction translator according to claim 8, wherein said translator translates the read out instruction in said second instruction architecture into the plurality of instructions as the instruction in said first instruction architecture (see Col.12 lines 42-56), but has not explicitly taught where said controller provides said first condition with one of said plurality of instructions and said second condition with each of said plurality of instructions but said one instruction.

34. However, Schacham has taught that a cache invalidation instruction can be executed to invalidate the entire instruction cache or a portion of it (see p.4 lines 28-30) in order to maintain proper cache coherence and provide better processor performance (see p.2 lines 8-23). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction cache of Emma in view of Gregor to allow a cache invalidation instruction to be executed so that cache coherency is maintained and processor performance is improved.

35. Emma in view of Gregor in view of Schacham has taught the invalidation of instructions in a cache based upon one of two conditions, namely a holding control condition as taught by Gregor, and a cache invalidation instruction as taught by Schacham. One of ordinary skill in the art would have recognized that because some instructions will have the first condition associated with them, and others will have the second condition associated with them. Therefore, one of ordinary skill in the art would have found it obvious that the processor of Emma in view of Gregor in view of Schacham will provide one instruction with a first condition, and other instructions with a second condition.

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36. Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665, as applied to claims 1 and 18 above.

37. Regarding claim 5, Emma has taught the instruction translator according to claim 1, wherein said translator includes a plurality of translators which translate a plurality of instruction in said second instruction architecture read out from said instruction memory into one instruction in said first instruction architecture (see Col.3 lines 2-17). While a plurality of translators is not explicitly taught, the translation of a plurality of instructions in the second instruction architecture into one instruction in the first instruction architecture is taught. The inclusion of a plurality of translators to perform the same function as a single translator provides no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the translator, creating a plurality of translators for translating instructions in a second instruction architecture into a single instruction in a first instruction architecture (see *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

38. Regarding claim 19, Emma has taught the data processing apparatus according to claim 16, further comprising a second instruction memory (604 of Fig.6) with a translator interconnected to said processor through said bus, said second instruction memory with a translator including:

- a. An instruction storage unit (604 of Fig.6) to store an instruction in a second instruction architecture different from said second instruction architecture, said instruction in said third instruction architecture being transferred from said processor through said bus (see Col.12 lines 51-56),

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- b. An instruction translation circuit responsive to an address signal applied from said processor through said bus, for translating an instruction in said third instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor (see Col.12 lines 59-67 and Col.13 lines 1-6).

39. Emma has not explicitly taught a third instruction memory with a translator for translating a third instruction architecture into a first instruction architecture is not explicitly taught.

40. However, adding a third instruction memory and corresponding third instruction architecture provides no new or unexpected result over the prior art except for allowing the additional translation of a third instruction architecture. But this could be achieved simply by replacing the second instruction architecture with the third architecture, as there are no claim limitations that require the two instruction architectures to be translated simultaneously.

Therefore, one of ordinary skill in the art would have found it obvious to duplicate the hardware used to operate on a second instruction architecture as taught by Emma in order to operate on a third instruction architecture (see *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Response to Arguments

41. Applicant's arguments filed on 3/15/04 have been fully considered but they are not persuasive.

42. On page 10, the Applicant argues in regards to claims 1, 12 and 16, in essence:

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“Emma does not disclose or suggest ‘a selector ... for selectively outputting ... an instruction output by said translator and the corresponding instruction held in said instruction cache’ as recited in independent claim 1.”

43. However, Emma does in fact teach the above limitation (see Emma, Col.12 line 59 – Col.13 line 6) as cited in paragraph 17 of the previous office action, dated 12/15/03, as well as again in above paragraph 7. Here, although a physically separate “selector” has not been explicitly taught, there is inherently some circuitry involved in the selection between the instruction coming from the EI-Cache and the I-Cache, such as the priority circuitry that chooses one instruction over the other based on which location it came from (see Emma, Col.12 line 59 – Col.13 line 6). Furthermore, in the second paragraph on p.11 of the present amendment, the Applicant even states, “In Emma, the processor may execute a conventional instruction or a translated instruction depending on whether the conventional instruction can be translated.” This is clearly a selection between a translated instruction and its corresponding non-translated instruction, as claimed in claim 1.

44. On page 11, the Applicant further argues in regards to claims 1, 12 and 16, in essence:

“One advantage of the claimed invention is that the processor receives instructions in the first instruction architecture and need not be capable of executing instructions in multiple instruction set architectures. Thus Emma does not disclose or suggest the claimed features of selecting an instruction in the first architecture from the translator or the instruction cache.”

45. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., selecting an

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instruction in the first architecture from the translator or the instruction cache) are not recited in the rejected claim(s). The claim simply recites, "selectively outputting ... an instruction output by said translator and the corresponding instruction held in said instruction cache. As shown above in paragraphs 7 and 43, Emma has taught the selective outputting of a translated instruction or its corresponding instruction held in the instruction cache. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

46. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the

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references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864.


The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
5/10/2004



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100